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EXAMINER	
DICKEY, THOMAS L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/840,173	Applicant(s) HAMAGUCHI ET AL.	
	Examiner Thomas L. Dickey	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed 2/9/06 has been entered.

Claim Objections

2. Applicant uses the claim terms "the memory functional element" and "the memory functional elements" extensively throughout the new and amended claims. There is no antecedent basis for these terms. Applicant apparently intended to use the terms "memory functional units," for which there is antecedent basis.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting

ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

A. Claims 8-13,19-23, and 29-33 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6, 8, and 20-23 of copending Application No. 10/846875 in view of LARSEN ET AL. (5,537,350) and MANABE ET AL. (2002/0040992).

(1) With regard to claims 8-13, Claims 1-6 and 8 of said copending application disclose a memory structure with (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion; (iii) a plurality of switching circuits for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) logic circuitry for enabling the plurality of switching circuits in a selected sequential order, wherein each of the side-wall memory transistors comprises: only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected

switching circuit of the plurality of switching circuits is connected to a selected set of the sets of bitlines, and said selected switching circuit of the plurality of switching circuits is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the logic circuitry comprises a state machine, the state machine enabling each of the plurality of switching circuits such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, and a bit line select circuit coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed.

With regard to claim 33, it is noted that on 3/17/06 Applicant amended said claim 1 of said co-pending application to include the language, "wherein the memory functional units have a structure selected from the group consisting of an insulating film including an insulator having the function of retaining charges, an insulating film including at least one conductor or semiconductor dot, and an insulating film including a ferroelectric film of which inner charge is polarized by an electric field and in which the polarized state is held" (emphasis added). Applicant apparently copied the underscored language verbatim from claims 28 and 33 of the amendment he submitted in the instant application on 2/9/06, barely five weeks before.

The language of claims 20-23 (added 3/17/06) of the co-pending application is an exact copy of the language of claims 29-32 (added 2/9/06) of the instant application,

except that co-pending claims 20-23 depend from copending claim 1. For this reason it may be said that claims 20-23 include all the limitations of claims 29-32 except as outlined below.

Claims 1-6 and 8 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation, that the plurality of switching circuits comprise four switching circuits, each switching circuit coupled to a corresponding set of four bitlines, or that a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

However, Larsen et al. discloses a memory structure with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a programming operation and a plurality switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Further, Manabe et al. teaches that it is easy and useful to perform a writing or erasing operation to a selected one of either of a pair of memory functional elements 124a, 124b formed on both sides of only a single gate electrode 122 independently from another operation performed on the other unselected memory functional element, by controlling each of three voltages:

1) the source voltage (or, in Applicant's long-winded way, the voltage applied to one of a pair of diffusion regions 126a, 126b) 2) the drain voltage (or, in Applicant's long-winded way, the voltage applied to the other of the diffusion regions 126a, 126b) and 3) the gate electrode. Note figures 1-3 (showing various memory structures) 4a-d (showing the applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed function) of Manabe et al. And of course Manabe et al. explains the value of this exercise is to be able to independently address the two bits stored in the pair of memory functional elements 124a and 124b. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said copending application's computer system with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and a plurality of means for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to thus provide a programmable EEPROM array with more reasonable current, and to perform the independent write/erase function advocated by Manabe et al. in order to independently address the separately stored bits.

(2) With regard to claims 19-23, claims 1-6 and 8 of said copending application disclose a structure for providing storage of data with (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall

memory transistor having a side-wall portion; (iii) a plurality of transferring means (switching circuits) for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) enabling means (logic circuitry) for enabling the plurality of transferring means (switching circuits) in a selected sequential order, wherein each of the side-wall memory transistors comprises: only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the enabling means (logic circuitry) comprises a state machine, the state machine enabling each of the plurality of transferring means (switching circuits) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed. Claims 1-6 and 8 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges

in each memory transistor during a programming operation, or that the plurality of means for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four switching circuits, a switching circuit is coupled to a corresponding set of four bitlines; set of four bitlines, or that a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

With regard to claim 33 (as said claim depends from claim 19), it is noted that on 3/17/06 Applicant amended said claim 1 of said co-pending application to include the language, "wherein the memory functional units have a structure selected from the group consisting of an insulating film including an insulator having the function of retaining charges, an insulating film including at least one conductor or semiconductor dot, and an insulating film including a ferroelectric film of which inner charge is polarized by an electric field and in which the polarized state is held" (emphasis added). Applicant apparently copied the underscored language verbatim from claims 28 and 33 of the amendment he submitted in the instant application on 2/9/06, barely five weeks before.

However, Larsen et al. discloses a structure for providing storage of data with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a programming operation and a plurality of means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a

corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Further, Manabe et al. teaches that it is easy and useful to perform a writing or erasing operation to a selected one of either of a pair of memory functional elements 124a, 124b formed on both sides of only a single gate electrode 122 independently from another operation performed on the other unselected memory functional element, by controlling each of three voltages: 1) the source voltage (or, in Applicant's long-winded way, the voltage applied to one of a pair of diffusion regions 126a, 126b) 2) the drain voltage (or, in Applicant's long-winded way, the voltage applied to the other of the diffusion regions 126a, 126b) and 3) the gate electrode. Note figures 1-3 (showing various memory structures) 4a-d (showing the applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed function) of Manabe et al. And of course Manabe et al. explains the value of this exercise is to be able to independently address the two bits stored in the pair of memory functional elements 124a and 124b. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said copending application's computer system with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and a plurality of means for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to thus provide

a programmable EEPROM array with more reasonable current, and to perform the independent write/erase function advocated by Manabe et al. in order to independently address the separately stored bits.

B. Claims 1-7, 14-18, and 28 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 10,11 and 13-15 of copending Application No. 10/846875 in view of LARSEN ET AL. (5,537,350) and MANABE ET AL. (2002/0040992).

(1) With regard to claims 1-7, claims 10,11, and 13-15 of said copending application disclose a computer system with (A) a CPU; (B) a structure for providing storage of data comprising (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion; (iii) a plurality of switching circuits for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) logic circuitry for enabling the plurality of switching circuits in a selected sequential order, wherein each of the side-wall memory transistors comprises: only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected switching circuit of the plurality of switching circuits is connected to a selected set of the sets of bitlines, and said selected

switching circuit of the plurality of switching circuits is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the logic circuitry comprises a state machine, the state machine enabling each of the plurality of switching circuits such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, and (C) a system bus means for transferring data and addresses between the CPU and the structure for providing storage of data.

With regard to claim 28 it is noted that on 3/17/06 Applicant amended each of said claims 10 and 11 of said co-pending application to include the language, "wherein the memory functional units have a structure selected from the group consisting of <u>an insulating film including an insulator having the function of retaining charges, an insulating film including at least one conductor or semiconductor dot, and an insulating film including a ferroelectric film of which inner charge is polarized by an electric field and in which the polarized state is held</u>" (emphasis added). Applicant apparently copied the underscored language <u>verbatim</u> from claims 28 and 33 of the amendment he submitted in the instant application on 2/9/06, barely five weeks before.

Claims 10,11, and 13-15 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation, or that the plurality of switching circuits comprise four switching circuits, each switching circuit coupled to a corresponding set of four bitlines; and a bit line select circuit coupled to the switching circuit to select bitlines of a set to

connect to receive the voltage such that the selected bitlines are programmed; or that a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

However, Larsen et al. discloses a computer system with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a programming operation and a plurality switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Further, Manabe et al. teaches that it is easy and useful to perform a writing or erasing operation to a selected one of either of a pair of memory functional elements 124a, 124b formed on both sides of only a single gate electrode 122 independently from another operation performed on the other unselected memory functional element, by controlling each of three voltages: 1) the source voltage (or, in Applicant's long-winded way, the voltage applied to one of a pair of diffusion regions 126a, 126b) 2) the drain voltage (or, in Applicant's long-winded way, the voltage applied to the other of the diffusion regions 126a, 126b) and 3) the gate electrode. Note figures 1-3 (showing various memory structures) 4a-d (showing the applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed

function) of Manabe et al. And of course Manabe et al. explains the value of this exercise is to be able to independently address the two bits stored in the pair of memory functional elements 124a and 124b. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said copending application's computer system with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and a plurality of means for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to thus provide a programmable EEPROM array with more reasonable current, and to perform the independent write/erase function advocated by Manabe et al. in order to independently address the separately stored bits.

(2) With regard to claims 14-18, claims 10,11, and 13-15 of said copending application disclose a computer system with (A) central processing means (a CPU); (B) means (structure) for providing storage of data comprising (i) a side-wall memory array including a plurality of side-wall memory transistors and sets of bitlines, each side-wall memory transistor having a side-wall portion; (iii) a plurality of transferring means (switching circuits) for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array; and (iv) enabling means (logic circuitry) for enabling the plurality of transferring means (switching circuits) in a selected sequential order, wherein each of the side-wall memory transistors comprises: only a single gate

electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, and wherein the side-wall memory transistors are in sets and wherein selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of side-wall memory transistors to be programmed, until the set of side-wall memory transistors to be programmed has been programmed and the enabling means (logic circuitry) comprises a state machine, the state machine enabling each of the plurality of transferring means (switching circuits) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, and (C) a system bus means for transferring data and addresses between the central processing means and the means (structure) for providing storage of data. Claims 10,11, and 13-15 of said copending application do not disclose a charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation, or that the plurality of means for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four switching circuits, each switching circuit coupled to a

corresponding set of four bitlines; or that a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

However, Larsen et al. discloses a computer system with a charge pump 30 for providing a voltage to accumulate negative charges in memory transistors during a programming operation and a plurality of means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four (44,45,46, and 47) switching circuits coupled to a corresponding set of four bitlines (seen without part # in figure 4, note column 8 line 11). Note figures 2-4, column 7 lines 7-40, and column 8 lines 4-17 of Larsen et al. Further, Manabe et al. teaches that it is easy and useful to perform a writing or erasing operation to a selected one of either of a pair of memory functional elements 124a, 124b formed on both sides of only a single gate electrode 122 independently from another operation performed on the other unselected memory functional element, by controlling each of three voltages: 1) the source voltage (or, in Applicant's long-winded way, the voltage applied to one of a pair of diffusion regions 126a, 126b) 2) the drain voltage (or, in Applicant's long-winded way, the voltage applied to the other of the diffusion regions 126a, 126b) and 3) the gate electrode. Note figures 1-3 (showing various memory structures) 4a-d (showing the applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed function) of Manabe et al. And of course Manabe et al. explains the value of this

exercise is to be able to independently address the two bits stored in the pair of memory functional elements 124a and 124b. Therefore, it would have been obvious to a person having skill in the art to augment claims 1-6 and 8 of said copending application's computer system with the charge pump for providing a voltage to accumulate negative charges in each memory transistor during a programming operation and a plurality of means for transferring the voltage to selected sets of a sets of bitlines of a memory array comprising four switching circuits coupled to a corresponding set of four bitlines such as taught by Larsen et al. in order to reduce the amount of current used in programming flash EEPROM memory arrays to thus provide a programmable EEPROM array with more reasonable current, and to perform the independent write/erase function advocated by Manabe et al. in order to independently address the separately stored bits.

C. Claims 24-27 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 10 and 11 of copending Application No. 10/846875 in view of LARSEN ET AL. (5,537,350) and MANABE ET AL. (2002/0040992), as applied to claims 1 and 14, above, and further in view of claims 20-23 of said copending Application No. 10/846875.

Claims 10 and 11 of copending Application No. 10/846875, Larsen et al. and Manabe et al. disclose a memory structure with all the limitations of claims 24-27 except that the pair of diffusion regions are disposed so as to offset with an end of the gate electrode, or to overlap with the memory functional element, wherein an overlap amount between the memory functional element and the diffusion region is 10 nm or more, and

a distance between an end of the gate electrode and an end of the diffusion region on the channel region side is less than 100 nm.

However, claims 20-23 of said copending Application No. 10/846875 disclose a memory structure wherein the pair of diffusion regions are disposed so as to offset with an end of the gate electrode, or to overlap with the memory functional element, an overlap amount between the memory functional element and the diffusion region being 10 nm or more and a distance between an end of the gate electrode and an end of the diffusion region on the channel region side being less than 100 nm. Therefore, it would have been obvious to a person having skill in the art to augment the memory structure suggested by claims 10 and 11 of copending Application No. 10/846875, Larsen et al. and Manabe et al. with the pair of diffusion regions are disposed so as to offset with an end of the gate electrode, or to overlap with the memory functional element, wherein an overlap amount between the memory functional element and the diffusion region is 10 nm or more, and a distance between an end of the gate electrode and an end of the diffusion region on the channel region side is less than 100 nm, such as taught by claims 20-23 of said copending Application No. 10/846875 in order to facilitate writing and erasing the memory functional elements by biasing the gate against said diffusion regions to thus provide faster and more accurate access to the data stored in said memory functional elements.

This is a <u>provisional</u> obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-25,28-30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over LARSEN ET AL. (5,537,350) in view of MANABE ET AL. (2002/0040992).

A. With regard to claims 1-7,24,25,27, and 28 Larsen et al. discloses a computer system with (A) a CPU 11 (central processor unit); (B) a memory arrangement comprising (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) logic circuitry 42 for enabling the plurality of switching circuits 44,45,46, and 47 in a selected sequential order, wherein the memory transistors 28 are in sets and wherein (one selected circuit out of the plurality of switching circuits 44,45,46, and 47 is connected to a selected set of the sets of bitlines, and said selected switching circuit of the plurality of switching circuits 44,45,46, and 47 is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set

of the sets of memory transistors 28 to be programmed, until the set of memory transistors 28 to be programmed has been programmed and the logic circuitry 42 comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2); the state machine enabling each of the plurality of switching circuits 44,45,46, and 47 such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47; a switching circuit is coupled to a corresponding set of four bitlines; a bit line select circuit (seen without part # in figure 4, note column 8 line 11). coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed; and (C) a system bus 12 for transferring data and addresses between the CPU 11 and the memory arrangement. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected

memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode. With further regard to claims 24,25,27 and 28 Larsen et al. does not disclose that the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot.

However, Manabe et al. discloses a computer system with memory transistors each having a side-wall portion (122A or 122B in figures 1 and 3) and comprising only a single gate electrode 122 formed on a semiconductor layer 100 with a gate insulating film 121 formed on the semiconductor layer 100; a channel region 110 formed below the gate electrode 122; a pair of diffusion regions 126A-B formed on the both sides of the channel region 110 and having a conductive type (N+) opposite to that (P-) of the channel region 110; and a pair of memory functional units 125A-B formed on the both sides of the gate electrode 122 and having a function of retaining charges (see, e.g., paragraph 0011), wherein a writing or erasing operation(see, e.g., paragraph 0012) to a selected one of either of the memory functional units 125A-B formed on both sides of the gate electrode 122 can be executed independently from the other unselected one of the memory functional units 125A-B by controlling each voltage applied to the diffusion regions 126A-B and the gate electrode 122, wherein the pair of diffusion regions 126A-B are disposed so as to either offset with an end of the gate electrode 122 (note figure 2) or overlap with the memory functional units 125A-B (note figure 1) and that the memory functional units 125A-B are formed by an insulating film 123A-B including at

least one conductor or semiconductor dot (124A or 124B). With particular regard to claim 27 note that in figure 1 note that the distance between an end of gate 122 and an end of diffusion region 126A is negative (they overlap) and thus less than 100 nm. Note figures 1-3 (showing various memory structures) 4a-d (showing the applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed function) of Manabe et al. Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s computer system with the memory transistors having side-wall portions and comprising only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode wherein the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot, such as taught by Manabe et al. in order to allow the

write cycle to reference drain 21 or source 20 and memory functional unit 18 during write operations to thus provide better more efficient write operation.

B. With regard to claims 8-13,29,30,32 and 33 Larsen et al. discloses a memory structure with (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) logic circuitry 42 for enabling the plurality of switching circuits 44,45,46, and 47 in a selected sequential order, wherein the memory transistors 28 are in sets and wherein (one selected circuit out of the plurality of switching circuits 44,45,46, and 47 is connected to a selected set of the sets of bitlines, and said selected switching circuit of the plurality of switching circuits 44,45,46, and 47 is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of memory transistors 28 to be programmed, until the set of memory transistors 28 to be programmed has been programmed and the logic circuitry 42 comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2), the state machine enabling each of the plurality of switching circuits 44,45,46, and 47 such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of switching circuits 44,45,46, and 47 for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47, a

switching circuit is coupled to a corresponding set of four bitlines; and further comprising a bit line select circuit (seen without part # in figure 4, note column 8 line 11). coupled to the switching circuit to select bitlines of a set to connect to receive the voltage such that the selected bitlines are programmed. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode. With further regard to claims 29,30, and 33 Larsen et al. does not disclose that the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot.

However, Manabe et al. discloses a memory structure with memory transistors each having a side-wall portion (122A or 122B in figures 1 and 3) and comprising only a single gate electrode 122 formed on a semiconductor layer 100 with a gate insulating

film 121 formed on the semiconductor layer 100; a channel region 110 formed below the gate electrode 122; a pair of diffusion regions 126A-B formed on the both sides of the channel region 110 and having a conductive type (N+) opposite to that (P-) of the channel region 110; and a pair of memory functional units 125A-B formed on the both sides of the gate electrode 122 and having a function of retaining charges (see, e.g., paragraph 0011), wherein a writing or erasing operation(see, e.g., paragraph 0012) to a selected one of either of the memory functional units 125A-B formed on both sides of the gate electrode 122 can be executed independently from the other unselected one of the memory functional units 125A-B by controlling each voltage applied to the diffusion regions 126A-B and the gate electrode 122, wherein the pair of diffusion regions 126A-B are disposed so as to either offset with an end of the gate electrode 122 (note figure 2) or overlap with the memory functional units 125A-B (note figure 1) and that the memory functional units 125A-B are formed by an insulating film 123A-B including at least one conductor or semiconductor dot (124A or 124B). With particular regard to claim 32 note that in figure 1 note that the distance between an end of gate 122 and an end of diffusion region 126A is negative (they overlap) and thus less than 100 nm. Note figures 1-3 (showing various memory structures) 4a-d (showing the applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed function) of Manabe et al. Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s memory structure with the memory transistors having side-wall portions and comprising only a single gate electrode formed on a

semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode wherein the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot, such as taught by Manabe et al. in order to allow the write cycle to reference drain 21 or source 20 and memory functional unit 18 during write operations to thus provide better more efficient write operation.

C. With regard to claims 14-18,24,25,27 and 28 Larsen et al. discloses a computer system with (A) central processing means (CPU 11); (B) means (structure) for providing storage of data comprising (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) enabling means (logic

circuitry 42) for enabling the plurality of transferring means (switching circuits 44,45,46, and 47) in a selected sequential order, wherein the memory transistors 28 are in sets and wherein selected transferring means (one selected circuit out of 44,45,46, and 47) of the plurality of transferring means (switching circuits 44,45,46, and 47) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits 44,45,46, and 47) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of memory transistors 28 to be programmed, until the set of memory transistors 28 to be programmed has been programmed and the enabling means (logic circuitry 42) comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2), the state machine enabling each of the plurality of transferring means (switching circuits 44,45,46, and 47) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47, a switching circuit is coupled to a corresponding set of four bitlines; and (C) a system bus 12 means for transferring data and addresses between the central processing means and the means (structure) for providing storage of data. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the

semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode. With further regard to claims 24,25, and 28 Larsen et al. does not disclose that the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot.

However, Manabe et al. discloses a computer system with memory transistors each having a side-wall portion (122A or 122B in figures 1 and 3) and comprising only a single gate electrode 122 formed on a semiconductor layer 100 with a gate insulating film 121 formed on the semiconductor layer 100; a channel region 110 formed below the gate electrode 122; a pair of diffusion regions 126A-B formed on the both sides of the channel region 110 and having a conductive type (N+) opposite to that (P-) of the channel region 110; and a pair of memory functional units 125A-B formed on the both sides of the gate electrode 122 and having a function of retaining charges (see, e.g., paragraph 0011), wherein a writing or erasing operation(see, e.g., paragraph 0012) to a selected one of either of the memory functional units 125A-B formed on both sides of

the gate electrode 122 can be executed independently from the other unselected one of the memory functional units 125A-B by controlling each voltage applied to the diffusion regions 126A-B and the gate electrode 122, wherein the pair of diffusion regions 126A-B are disposed so as to either offset with an end of the gate electrode 122 (note figure 2) or overlap with the memory functional units 125A-B (note figure 1) and that the memory functional units 125A-B are formed by an insulating film 123A-B including at least one conductor or semiconductor dot (124A or 124B). With particular regard to claim 27 note that in figure 1 note that the distance between an end of gate 122 and an end of diffusion region 126A is negative (they overlap) and thus less than 100 nm. Note figures 1-3 (showing various memory structures) 4a-d (showing the applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed function) of Manabe et al.

Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s computer system with the memory transistors having side-wall portions and comprising only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected

memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode wherein the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot, such as taught by Manabe et al. in order to allow the write cycle to reference drain 21 or source 20 and memory functional unit 18 during write operations to thus provide better more efficient write operation.

D. With regard to claims 19-23,29,30,32, and 33 Larsen et al. discloses a structure for providing storage of data with (i) a memory array including a plurality of memory transistors 28 and sets of bitlines (seen without part # in figure 4, note column 8 line 11); (ii) a charge pump 22 for providing a voltage to accumulate negative charges in the portion of each memory transistor during a programming operation; (iii) a plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of the sets of bitlines of the memory array; and (iv) enabling means (logic circuitry 42) for enabling the plurality of transferring means (switching circuits 44,45,46, and 47) in a selected sequential order, wherein the memory transistors 28 are in sets and wherein selected transferring means (one selected circuit out of 44,45,46, and 47) of the plurality of transferring means (switching circuits 44,45,46, and 47) is connected to a selected set of the sets of bitlines, and said selected transferring means (switching circuit) of the plurality of transferring means (switching circuits 44,45,46, and 47) is enabled to transfer a first voltage to the selected set of the sets of bitlines, the selected set being coupled to a set of the sets of memory transistors 28 to be programmed, until

the set of memory transistors 28 to be programmed has been programmed and the enabling means (logic circuitry 42) comprises a state machine (note figure 4 and column 8 lines 18-25, also see claim 2), the state machine enabling each of the plurality of transferring means (switching circuits 44,45,46, and 47) such that the voltage is applied individually to the sets of bitlines until each set of the sets of bitlines has been programmed, the plurality of transferring means (switching circuits 44,45,46, and 47) for transferring the voltage to selected sets of the sets of bitlines of the side-wall memory array comprise four (44,45,46, and 47) switching circuits 44,45,46, and 47, a switching circuit is coupled to a corresponding set of four bitlines. Note figures 1-4, column 7 lines 7-40, and column 8 lines 4-25 of Larsen et al. Larsen et al. does not disclose that each memory transistor has a side-wall portion and comprises only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode. With further regard to claims 29,30, and 33 Larsen et al. does not disclose that the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and

overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot.

However, Manabe et al. discloses a structure for providing storage of data with memory transistors each having a side-wall portion (122A or 122B in figures 1 and 3) and comprising only a single gate electrode 122 formed on a semiconductor layer 100 with a gate insulating film 121 formed on the semiconductor layer 100; a channel region 110 formed below the gate electrode 122; a pair of diffusion regions 126A-B formed on the both sides of the channel region 110 and having a conductive type (N+) opposite to that (P-) of the channel region 110; and a pair of memory functional units 125A-B formed on the both sides of the gate electrode 122 and having a function of retaining charges (see, e.g., paragraph 0011), wherein a writing or erasing operation (see, e.g., paragraph 0012) to a selected one of either of the memory functional units 125A-B formed on both sides of the gate electrode 122 can be executed independently from the other unselected one of the memory functional units 125A-B by controlling each voltage applied to the diffusion regions 126A-B and the gate electrode 122, wherein the pair of diffusion regions 126A-B are disposed so as to either offset with an end of the gate electrode 122 (note figure 2) or overlap with the memory functional units 125A-B (note figure 1) and that the memory functional units 125A-B are formed by an insulating film 123A-B including at least one conductor or semiconductor dot (124A or 124B). With particular regard to claim 32 note that in figure 1 note that the distance between an end of gate 122 and an end of diffusion region 126A is negative (they overlap) and thus less than 100 nm. Note figures 1-3 (showing various memory structures) 4a-d (showing the

applied voltages) 8 (showing a way to independently write to one and then the other memory element) and 10 (showing the circuitry needed to accomplish the claimed function) of Manabe et al.

Therefore, it would have been obvious to a person having skill in the art to replace the memory transistors of Larsen et al.'s structure for providing storage of data with the memory transistors having side-wall portions and comprising only a single gate electrode formed on a semiconductor layer with a gate insulating film formed on the semiconductor layer; a channel region formed below the gate electrode; a pair of diffusion regions formed on the both sides of the channel region and having a conductive type opposite to that of the channel region; and a pair of memory functional units formed on the both sides of the gate electrode and having a function of retaining charges, wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode wherein the pair of diffusion regions are disposed so as to offset with an end of the gate electrode and overlap with the memory functional element or that the memory functional element is formed by an insulating film including at least one conductor or semiconductor dot, such as taught by Manabe et al. in order to allow the write cycle to reference drain 21 or source 20 and memory functional unit 18 during write operations to thus provide better more efficient write operation.

Response to Arguments

5. Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
04/06